

## CLAIMS

What is claimed is:

- 1 1. A method for adaptively compressing test data to be provided to a device under test  
2 (DUT), the method comprising the steps of:  
3       examining a test data file that includes a first plurality of data units corresponding to a  
4       first plurality of DUT pins and a second plurality of data units corresponding to a  
5       second plurality of DUT pins;  
6       compressing the first plurality of data units using a first compression technique; and  
7       compressing the second plurality of data units using a second compression technique.
- 1 2. The method of claim 1, further comprising, prior to the steps of compressing:  
2       determining a timing complexity for the first plurality of data units; and  
3       determining a timing complexity for the second plurality of data units.
- 1 3. The method of claim 1, wherein the first plurality of data units corresponds to clock signals  
2 and the second plurality of data units corresponds to non-clock signals.
- 1 4. The method of claim 1, wherein compressing the first plurality of data units by a  
2 predetermined compression rate requires more resources than compressing the second  
3 plurality of data units by the predetermined compression rate.
- 1 5. The method of claim 1, wherein the first plurality of data units have a different timing  
2 complexity than the second plurality of data units.
- 1 6. The method of claim 1, wherein the first plurality of data units have a different vector data  
2 volume than the second plurality of data units.
- 1 7. The method of claim 1, wherein the first plurality of data units have more repetitive data  
2 patterns than the second plurality of data units.

1 8. The method of claim 1, wherein the first plurality of DUT pins are clock-pins and the  
2 second plurality of DUT pins are non-clock-pins.

1 9. The method of claim 1, further comprising the step of:  
2 formatting the first plurality of data units independently from the second plurality of data  
3 units.

1 10. The method of claim 1, wherein the test data file is one of a STIL (standard test interface  
2 language) file and a WGL (waveform generation language) file.

1 11. The method of claim 1, wherein at least one processor operating in a first timing domain  
2 enables the first plurality of data units to be provided to the first plurality of DUT pins, and at  
3 least one processor operating in a second timing domain enables second plurality of data units  
4 to be provided to the second plurality of DUT pins, wherein the second timing domain is  
5 different from the first timing domain.

1 12. A method for adaptively compressing test data to be provided to a device under test  
2 (DUT), the method comprising the steps of:  
3 examining a test data file that includes test data configured to enable testing the DUT,  
4 the test data file including a first plurality of data units and a second plurality of  
5 data units, the first plurality of data units corresponding to a first plurality of  
6 DUT pins, and the second plurality of data units corresponding to a second  
7 plurality of DUT pins;  
8 determining that the first plurality of data units have a first compressibility characteristic;  
9 and  
10 determining that the second plurality of data units have a second compressibility  
11 characteristic.

1 13. The method of claim 12, further comprising the step of:  
2 compressing the first plurality of data units independently from the second plurality of  
3 data units.

1 14. The method of claim 12, wherein the first plurality of DUT pins are clock-pins and the  
2 second plurality of DUT pins are non-clock-pins.

1 15. The method of claim 12, wherein the test data file is one of a STIL (standard test  
2 interface language) file and a WGL (waveform generation language) file.

1 16. The method of claim 12, wherein the first plurality of data units have a different timing  
2 complexity, a different vector data volume, and more repetitive data patterns than the second  
3 plurality of data units.

1 17. A system for adaptively compressing test data to be provided to a device under test (DUT),  
2 the system comprising:  
3 memory configured to store a test data file that includes a first plurality of data units  
4 corresponding to a first plurality of DUT pins and a second plurality of data units  
5 corresponding to a second plurality of DUT pins; and  
6 a processor operative to:  
7 compress the first plurality of data units using a first compression technique; and  
8 compress the second plurality of data units using a second compression  
9 technique.

1 18. The system of claim 17, wherein the processor is operative to:  
2 determine a timing complexity for the first plurality of data units; and  
3 determine a timing complexity for the second plurality of data units.

1 19. The system of claim 17, wherein the first plurality of data units correspond to clock signals  
2 and the second plurality of data units correspond to non-clock signals.

1 20. The system of claim 17, wherein compressing the first plurality of data units by a  
2 predetermined compression rate requires more resources than compressing the second  
3 plurality of data units by the predetermined compression rate.

1 21. The system of claim 17, wherein the first plurality of data units have a different timing  
2 complexity than the second plurality of data units.

1 22. The system of claim 17, wherein the first plurality of data units have a different vector  
2 data volume than the second plurality of data units.

1 23. The system of claim 17, wherein the first plurality of data units have more repetitive data  
2 patterns than the second plurality of data units.

1 24. The system of claim 17, wherein the first plurality of DUT pins are clock-pins and the  
2 second plurality of DUT pins are non-clock-pins.

1 25. The system of claim 17, further comprising the step of:  
2 formatting the first plurality of data units independently from the second plurality of data  
3 units.

1 26. The system of claim 17, wherein the test data file is one of a STIL (standard test interface  
2 language) file and a WGL (waveform generation language) file.

1 27. The system of claim 17, wherein at least one processor operating in a first timing domain  
2 enables the first plurality of data units to be provided to the first plurality of DUT pins, and at  
3 least one processor operating in a second timing domain enables the second plurality of data  
4 units to be provided to the second plurality of DUT pins, wherein the second timing domain  
5 is different from the first timing domain.

1 28. A system for adaptively compressing test data to be provided to a device under test (DUT),  
2 the system comprising:

3 memory configured to store a test data file that includes test data configured to enable  
4 testing the DUT, the test data file including a first plurality of data units and a  
5 second plurality of data units, the first plurality of data units corresponding to a  
6 first plurality of DUT pins, and the second plurality of data units corresponding  
7 to a second plurality of DUT pins; and

8 a processor that is operative to:

9 determine that the first plurality of data units have a first compressibility  
10 characteristic;

11 determine that the second plurality of data units have a second compressibility  
12 characteristic.

1 29. The system of claim 28, wherein the processor is operative to:

2 compress the first plurality of data units independently from the second plurality of  
3 data units.

1 30. The system of claim 28, wherein the first plurality of DUT pins are clock-pins and the  
2 second plurality of DUT pins are non-clock-pins.

1 31. The system of claim 28, wherein the test data file is one of a STIL (standard test interface  
2 language) file and a WGL (waveform generation language) file.

1 32. The system of claim 28, wherein the first plurality of data units have a different timing  
2 complexity, a different vector data volume, and more repetitive data patterns than the second  
3 plurality of data unit